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**AMENDMENTS TO THE DRAWINGS**

Please replace drawing pages 1-7, 9 and 13 currently on file in this application with replacement pages enclosed herewith. Pages 1-6 containing Figures 1-8, page 9 containing Figures 15-17 and page 13 containing Figures 27 and 28 are replaced to improve the quality of the drawings. Page 7 containing Figures 9-11 is replaced to correct a typographical error in which reference numbers (14a) pointing to clocked transistors 18a and 18b are corrected to read --14b--.

Attachment: Replacement Sheets  
Annotated Sheets showing Changes.

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### REMARKS/ARGUMENTS

Reconsideration of this application is respectfully requested.

#### *Drawings*

The Office Action objected to the drawings because lines, numbers and letters in Figures 1-28 were considered to lack uniformity and definition. Pages 1-6, 9 and 13 of the drawings are replaced. Page 7 is replaced to correct a typographical error in which the reference number "14a" generally indicating the n-mosfet transistors 18a and 18b is corrected to read --14b-- to accord with the description as originally filed.

It is respectfully submitted that drawings as amended comply with 37 CFR 1.84(1).

#### *Claim Rejections - 35 USC § 102*

The Office Action rejected claims 1 and 3-12 under 35 USC § 102(b) as being anticipated by Nakajima. Nakajima teaches a clock-control gate circuit that employs field-effect transistors of both n- and p-type conductivities. The circuit includes a precharged circuit, a logic circuit and a switching transistor serially connected in that order between a power source and ground in a capacitor connected to the junction between the precharged circuit and the logic circuit. In accordance with Nakajima, the precharged circuit includes only n-type transistors whereas the switching transistor comprises only p-type transistors. Claim 1 is cancelled and the rejection is traversed.

The subject matter of claim 1 is incorporated into amended claim 2 and the rejection of claims 2-8 is likewise traversed.

Claim 9 is amended to claim that the evaluate clock logic circuit comprises first and second n-mosfet transistors. This clearly distinguishes over the teachings of Nakajima and the rejection of claims 9-12 is traversed.

New claims 13-20 are added to the application. New claim 13 claims a single-rail multi-gate domino logic circuit driven by a multi-phase clock comprising a first dynamic logic stage comprising a precharge clock logic circuit comprising at least one p-mosfet transistor respectively driven by a separate phase of the multi-phase clock and a second dynamic logic stage comprising an evaluate clock logic circuit comprising at least one n-mosfet transistor respectively driven by a separate phase of the multi-phase clock. This likewise clearly distinguishes over the teachings of Nakajima and it is respectfully submitted that claims 13-20 claim novel and inventive subject matter.

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***Claim Rejections - 35 USC § 103a***

The Office Action rejected claim 2 as being unpatentable over Nakajima applied to claim 1 above and further in view of Kumar. Applicant respectfully disagrees.

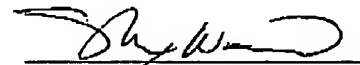
As acknowledged in the Office Action, Kumar teaches PMOS (25 in Fig. 10a) that is replaced with an inverter and a NMOS for the purpose of providing faster speed (col. 7, line 56+).

However, none of the circuits taught or claimed in the instant invention include an inverter. Consequently, Nakajima in combination with Kumar teach away from the invention claimed in claims 1-20 now pending in this application. As explained in paragraphs [0044]-[0066], the purpose of using PMOS devices for the precharge function and NMOS devices for the evaluate function is to prevent overlap between the precharge of one logic cell and the evaluation of an adjacent cell, a problem not addressed by Nakajima or Kumar.

In view of these amendments and for reasons set forth above, this application is now considered to be in a condition for immediate allowance. Favourable reconsideration and early issuance of a Notice of Allowance is requested.

Respectfully submitted,

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## APPENDIX A